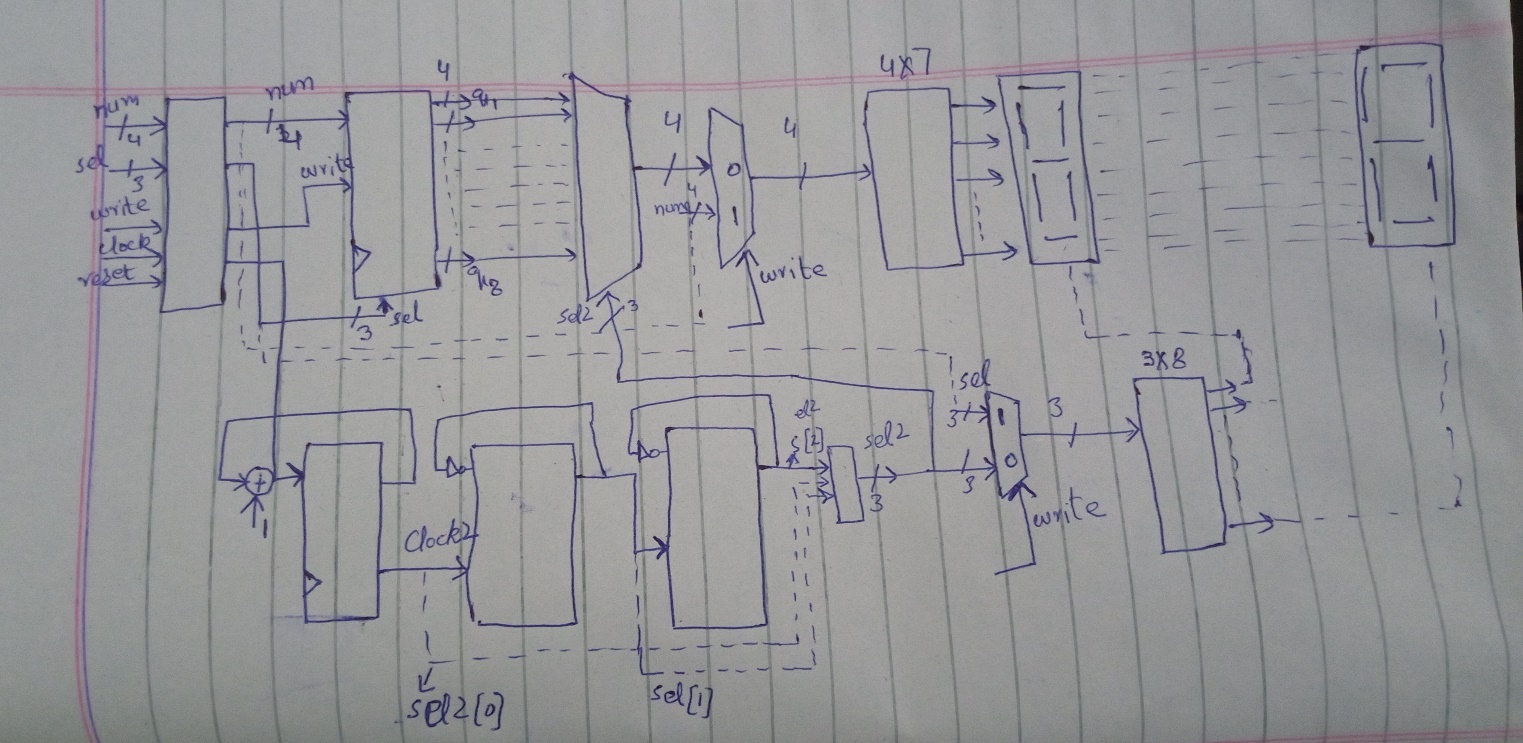
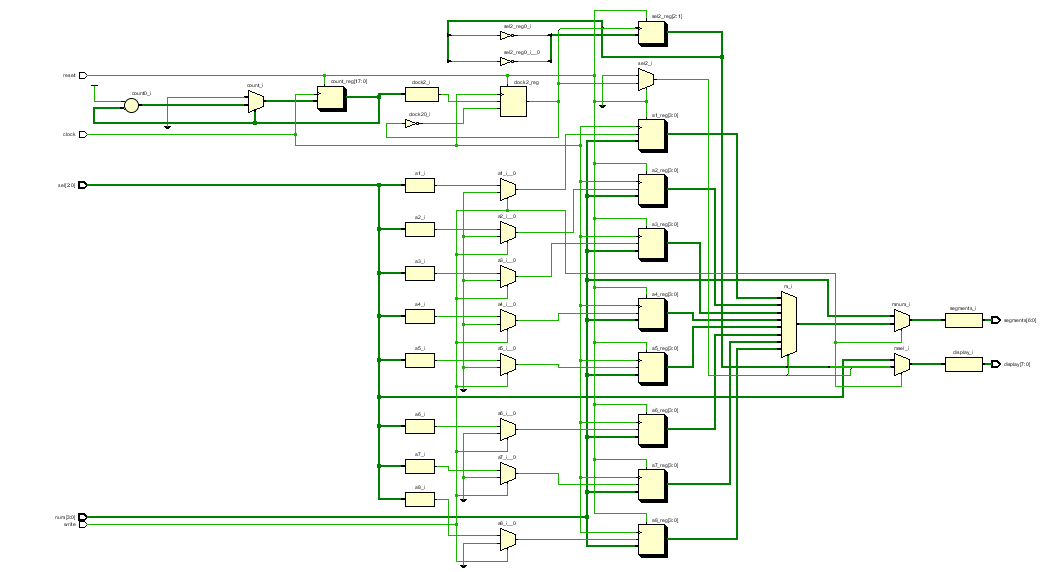
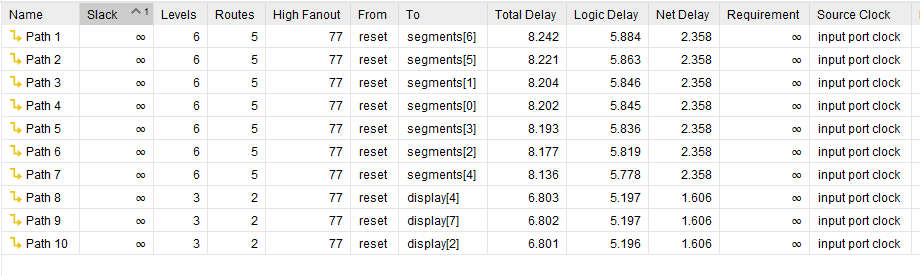
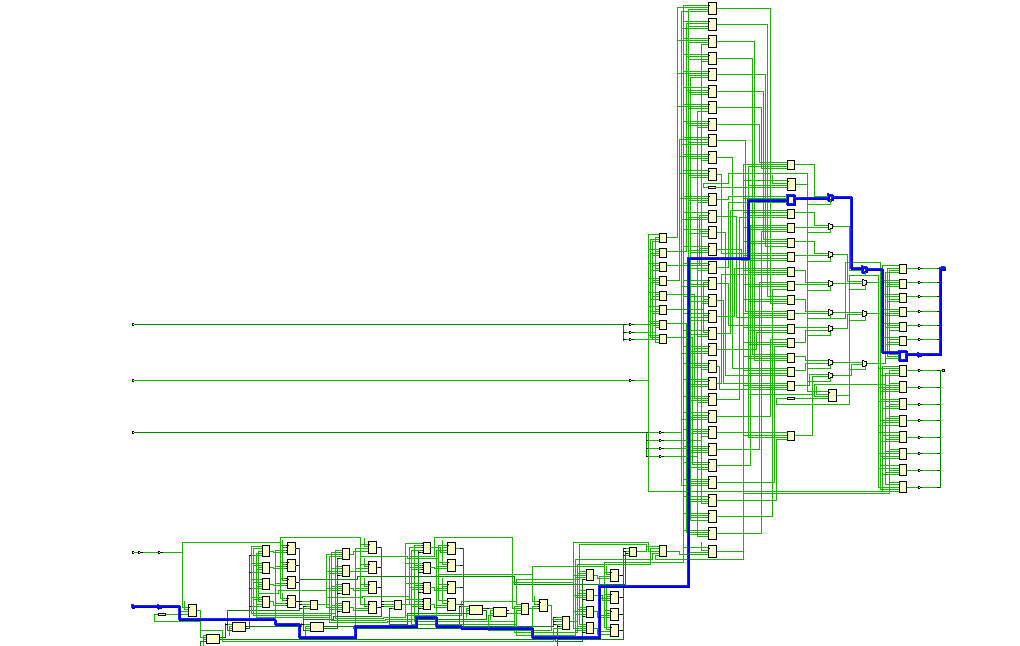
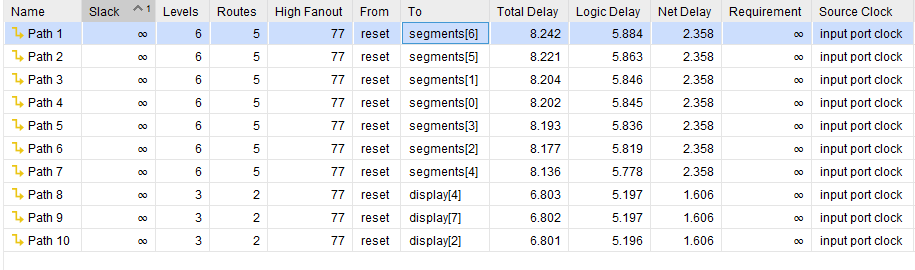
|  |  |
| --- | --- |
| Name: Muhammad Boota | EE-272L Digital Systems Design |
| Reg. No.: 2022-EE-134 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**Lab Report**

**Lab 6**

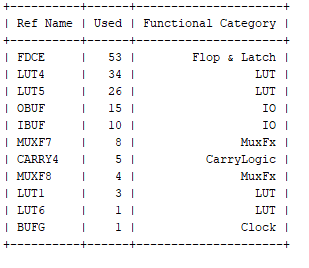
1. circuit design:
2. hand sketched
3. Schematic diagram
4. Synthesis maximum combinational delay.

Path (from reset to segment [6]) has the maximum synthesis combinational delay.

1. Implementation maximum combinational delay

Path (from reset to segment [6]) has the maximum implementation combinational delay which is same as maximum synthesis combinational delay.

1. Resource Utilization Report.



No. of LUTs=64.

No. of IOs=25.